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10/743,104	12/23/2003	Mitsuhiko Ogihara	MAE 305	8001

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EXAMINER	
MONDT, JOHANNES P	

ART UNIT	PAPER NUMBER
3663	

DATE MAILED: 12/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/743,104	OGIHARA ET AL.	
	Examiner	Art Unit	
	Johannes P. Mondt	3663	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 September 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-6,9,10,16-20,26-32,35 and 36* is/are pending in the application.

4a) Of the above claim(s) *19,26-32,35 and 36* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-6, 9-10, 16-18 and 20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election with traverse of Species 1 in the reply filed on 9/25/06 is acknowledged. The traversal is on the ground that Species 1 and Species 2 are "the same Species" (page 1 of response filed 9/25/06). This is not found persuasive because applicant does not address the Species as disclosed, merely the present claims. The Election Requirement mailed 8/28/06 was, however, based on the difference between Species 1 and Species 2 as disclosed, said difference residing in the single epi film bonded on each metal layer 105 with each LED epi film having a single LED in Species 2 and planarized film 104 disposed on planarized region 103 with LED epi film 110 in Species 1, introduced in Applicant's own Specification as different Embodiments 2 and 1, respectively. As explained in said Election of Species Requirement, bonding of epi films, planarization and elevations in layers are substantial and patentable limitations. Applicant does not address this point.

The requirement is still deemed proper and is therefore made FINAL.

Accordingly, claims 2-6, 9-10, 16-18 and 20 are being examined and claims 19, 26-32, 35 and 36 have been withdrawn from consideration.

Response to Amendment

Amendment filed 6/13/06 together with response to said election-of-species requirement forms the basis for this office action. In said Amendment applicant substantially amended all elected claims 2-6, 9-10, 16-18 and 20 through substantial amendment of independent claim 5. Comments on Remarks

submitted with said Amendment are included below under "Response to Arguments".

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. ***Claims 2, 4, 5 and 17*** are rejected under 35 U.S.C. 102(b) as being anticipated by Zhang et al (6,255,705 B1).

On independent claim 5: Zhang et al teach a combined semiconductor apparatus (see Figures 1E and 3B, and columns 7-16) comprising: a semiconductor substrate 101 (col. 11, l. 62-65) having an integrated circuit (CMOS circuit comprising transistors 151 and 152; Figure 1E and col. 8, l. 1-3) in a final structure that could have been obtained through formation of said integrated circuit in said semiconductor substrate; a semiconductor thin film (crystalline silicon film 125/126/127 resulting from 104) (col. 12, l. 3-8 and col. 8, l. 22-26) including at least one semiconductor device (namely the active region 126 of TFT 153; see Figure 1E and col. 7, l. 60-67) and bonded on a planar region (through said a planar film 102 (col. 11, l. 65 – col. 12, l. 9); and a planar film 102 disposed between said planar region (upper oxidized surface of semiconductor substrate 101) and said semiconductor thin film (125/126/127

resulting from 104) (see Figure 1E), said planar region being planar on the side of the semiconductor device (see Figure 1E).

The limitation "planarized" only has patentable weight in the device application of applicant to the extent the final structure is further limited by it. But the limitation "planarized" in "planarized region" and in "planarized film" (lines 4 and 7) does not carry patentable weight for the final structure, because whether a planarization step was carried out in an attempt to make a structure planar is only a limitation on the method of making said structure, and as such even only guarantees an attempt has been made to make said structure or layer planar.

Similarly, the limitation "wherein a surface of said planarized film on a side of said semiconductor thin film has been subjected to a planarizing process" does not further limit said planarized, i.e., planar, film so long as the planar surface of said planar film is on the side of the semiconductor device, which, as we have seen, is the case.

In conclusion, Zhang et al anticipate claim 5.

On claim 2: said planar region is a part of said surface of said semiconductor substrate (upper surface-oxidized surface of single-crystal silicon substrate 101). Again: whether a planarizing process has been carried out has no patentable weight in the present device invention, with reference to the discussion on this topic in the rejection of claim 5.

On claim 4: said planarized region is disposed in a region of said semiconductor substrate adjacent to (i.e., nearby) said integrated circuit of said

semiconductor substrate because TFTs 151, 152 are adjacent to TFT 153, being provided on the same substrate.

On claim 17: said at least one semiconductor apparatus is a light-emitting element (active matrix LCD) (col. 7, l. 49-44) and said integrated circuit 151/152 includes a driving-IC driving said at least one semiconductor device (col. 7, l. 48-52).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. ***Claims 3, 6 and 18*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Zhang et al as applied to claim 5, in view of Walker et al (6,841,813 B2).

On claim 6: As detailed above, Zhang et al anticipate claim 5. Zhang et al do not necessarily teach the further limitations defined by claim 6.

However, it would have been obvious to include said limitations *in view of Walker et al, who*, in a patent on integrated devices including TFTs (col. 1), hence analogous art, teach the stacking of TFT devices in three-dimensional arrays including a plurality of different vertical planar device levels 3A and 3B (abstract and Figures 1 and 4) (col. 4, l. 30-39 and col. 6, l. 47-53); see also first and second planar layers 26 and 27 (col. 5, l. 55-65) in Figure 5A. Because the

planarized film of the claim can be identified with any of the interlayer insulation films other than at the vertically highest level, e.g., with 3B, the claim limitation is met through the inclusion of the teaching by Walker et al of three-dimensional TFT mask ROM array with said planar layers, because planar film 3B is disposed between the planarized region formed by the upper main surface of the substrate and the semiconductor thin film of the TFT overlying said planar film 3B while 3B includes an electrically conductive layer, namely the gate layer of any of the TFTs in 3B, and 3B also includes an interlayer dielectric layer formed in a region peripheral, i.e., surrounding, said gate layer, namely the remainder of 3B (Figure 4B, e.g.). *Motivation* to include the teaching by Walker et al is their teaching of the reduction of the effective cell array through their three-dimensional array (col. 3, l. 3-10).

On claim 3: the above-described incorporation of the teaching by Walker et al implies a planar region disposed above an integrated circuit (any circuit integrated in the device on said semiconductor substrate that is located at a lower level than a planar region in a surface of one of the semiconductor channel layers 13 (Figure 3 and col. 5, l. 42) positioned at a level that is higher than said lower level).

On claim 18: in the combined invention according to Zhang et al with three-dimensional array levels implemented according to Walker et al a plurality of semiconductor devices are arranged in said semiconductor thin film 13 (see Figure 5A and col. 5, l. 41-43, for instance).

3. ***Claim 16*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Zhang et al as applied to claim 5, in view of Yamazaki et al (6,184,556 B1).

As detailed above, Zhang et al anticipate claim 5. Zhang et al do not necessarily teach said semiconductor thin film to be a compound semiconductor substrate as its main material. *However, SiGe, a compound semiconductor, has long been taught as preferable over silicon for its higher electron mobility, as witnessed by Yamazaki et al (see Third Embodiment, col. 15, l. 4-9). Motivation* for higher mobility of charge carriers is obvious because of the resulting faster response of the device. Moreover, it has been held that mere selection of known materials generally understood to be suitable to make a device, the selection of the particular material being on the basis of suitability for the intended use, would be entirely obvious. In re Leshin 125 USPQ 416.

4. ***Claim 20*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Zhang et al as applied to claim 5, in view of Hayashi et al (JP-09045930 A).

As detailed above, Zhang et al anticipate claim 5. Zhang et al do not necessarily teach the further limitation as defined by claim 20. However, it would have been obvious to include said further limitation in view of Hayashi et al, who teach the application of TFTs in active matrix displays for inter alia an optical printer head. It is thus seen that optical printer head applications are obvious applications of the active matrix display by Zhang et al. *Motivation* to include the

teaching by Hayashi et al immediately flows from the resulting enlargement of the range of applications.

5. ***Claims 5 and 9-10*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Zhang (US 2003/0067043 A1) in view of Muto et al (JP 61102767 A).

Zhang teaches a combined semiconductor apparatus (three-dimensional IC memory array integrated with an embedded read-write memory (eRWM): title, abstract and [0023]-[0024]) comprising: a substrate having an integrated circuit (0s) ([0074]) formed therein (0s comprises address decoder circuitry ([0074]); a semiconductor thin film (20a ([0109]) including at least one semiconductor device (P+/N-/N+ diode) and bonded on a planar region 30a (Figure 10BA); said planar region being defined on (not directly on, but nevertheless "on") a surface of said semiconductor substrate; and a planar film 23 (Figure 9A and [0101) disposed between said planar region and said semiconductor thin film.

Zhang teaches a combined semiconductor apparatus (three-dimensional IC memory array integrated with an embedded read-write memory (eRWM): title, abstract and [0023]-[0024]) comprising: a substrate having an integrated circuit (0s) ([0074]) formed therein (Os comprises address decoder circuitry (see again the recited paragraph [0074]); a semiconductor thin film (either 20a or 30a2: ([0109]) including at least one semiconductor device (P+/N-/N+ diode) and bonded on a planar region (Figure 10BA; in the case of 30a2 this bonding is indirect but present through 20a; for 20a it is either direct or indirect, as 20a can be seen in Figure 10BA to rest on a number of planar layers serving as its

substrates); and a planar film 23 (Figure 9A and [0101) disposed between said planar region and said semiconductor thin film.

The limitations "planarized" (lines 4 and 7) fail to further limit the planar region and planar film but instead only limit the method of making by describing a process step. Similarly, the limitation "wherein a surface of said planarized film on a side of said semiconductor thin film has been subjected to a planarizing process" does not further limit said planarized, i.e., planar, film so long as the planar surface of said planar film is on the side of the semiconductor device, which, as we have seen, is the case.

Zhang does not necessarily teach said substrate to be a semiconductor substrate. *However, as witnessed by Muto et al,* a compound semiconductor substrate of semi-insulating GaAs is advantageous because it allows read and write operations to be conducted at high speed (see English abstract). *Motivation,* to include the teaching by Muto et al, directly follows from the high read/write speed considering the eRWM component in the device by Zhang.

On claim 9: said semiconductor thin film as selected to be 30a2 has a common electrode layer 20a on a second surface of the semiconductor thin film opposed to a first surface of the semiconductor film, in which said semiconductor device is formed (first surface is upper main surface, second surface is lower main surface, of 30a2) (cf. Figure 10BA), and said second surface of said semiconductor thin film is disposed on a side of said planarized region of said semiconductor substrate (because said semiconductor substrate with planarized region is below said semiconductor thin film (cf. Figure 10BA).

On claim 10: said integrated circuit includes individual electrode terminals (source/drain terminal are inherent to the transistors 0T, etc. (Figure 2A); said apparatus further comprising individual interconnecting lines 20av, 30av,.., formed on a region extending from an upper surface of said semiconductor device to said individual electrode terminals (cf. Figure 2A and [0074]).

Response to Arguments

Applicant's arguments filed 6/13/06 have been fully considered but they are not persuasive.

Although examiner apologizes for confusion on Summary Form PTO-326 all claims 2-6, 9-10, 16-18 and 20 has been rejected with proper headings in office action mailed 3/2/06.

In particular, first with regard to arguments in traverse of rejections of claims 2, 4, 5 and 17 as being anticipated by Zhang et al (6,255,705): counter to applicant's allegation in apparent support of patentability of the invention that the claimed semiconductor apparatus "includes a semiconductor substrate having an integrated circuit formed therein" (page 8 of Remarks) in alleged contrast with Zhang et al, because "TFTs 151, 152, and 153 are formed over the substrate 101 and separated therefrom by the film 102, so that this reference does not disclose or suggest a semiconductor substrate having an integrated circuit formed therein, as recited by [amended] claim 5" (page 9 of Remarks), the First Embodiment as elected clearly and explicitly is limited to integrated circuit 102 being formed in a surface of said semiconductor substrate 101 ([0041]), while said surface is

invariably the upper main surface of said substrate in all drawings of said First Embodiment. See Figures 1-12. That the integrated circuit still is stated to be formed in the semiconductor (Si) substrate ([0046]) thus has at most implications for the manner in which said final structure is obtained. It is only because said integrated circuit *can* be formed in said semiconductor substrate that the subject matter of the new claims cannot be stated to introduce new matter. Indeed, all layers in Zhang pertaining to the TFT's 151, 152 and 153 are obtainable from the same initial material of which semiconductor substrate 101 is made, i.e., silicon: underlying layer 102 is only optional (see col. 7, l. 53-55), while gate layer 112 is made of impurity-imparted silicon (col. 7, l. 56-59), hence possible to manufacture from the silicon substrate 101 (e.g., col. 11, l. 62-65) by oxidation.

The limitations formed "therein" and "planarized" are only of patentable weight in as much as the method steps distinguish the final structure, and to the extent not impacting final structure are taken to be product-by-process limitations and non-limiting. A product by process claim is directed to the product per se, no matter how they are actually made. See In re Fessman, 180 USPQ 324, 326 (CCPA 1974); In re Marosi et al, 218 USPQ 289, 292 (Fed. Cir. 1983), and In re Thorpe, 227 USPQ 964, 966 (Fed. Cir. 1985), all of which make clear that it is the patentability of the final structure of the product "gleaned" from the process steps that must be determined in a "product-by-process" claim, and not the patentability of the process. See also MPEP 2113. Moreover, an old or obvious product produced by a new method is not a patentable product, whether claimed in "product by process" claims or not.

Accordingly, applicant's argument fails to persuade and the claims rejected over Zhang et al (6,255,705) again stand rejected over the same art as cited in the previous action on the merits.

Furthermore, traverse of rejections of claims 3, 6 and 18 over Zhang (loc.cit.) in view of Walker et al and of rejections of claims 16 and 20 over Zhang et al in view of Yamazaki et al and Hayashi et al, merely rely on aforementioned arguments in traverse of the rejections of claims 2, 4, 5 and 17.

On the arguments in traverse of the rejections of claims 5, 9 and 10 over Zhang (US 2003/0067043), the alluded difficulty "to ascertain which features of the Zhang reference the examiner is equating to be the equivalent of Applicant's claimed features" is not understood: the cited portions [0023]-[0024] recite substrate-IC's, i.e., "substrate integrated circuits" ([0023]), of which Os was cited specifically. It is thus clear that said IC is formed in or (directly) on a substrate while the distinction between "in" and "on" to the extent disclosed in the specification of applicant is of no patentable weight for the same reason as given above in response to the traverse of rejections based on Zhang (6,255,705). No specific other arguments including those in traverse of the arguments based on Muto other than discussed above appear to pertain to the elected claims.

Arguments in traverse of non-elected claims are moot since said non-elected claims have been withdrawn from consideration.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.**

See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P. Mondt whose telephone number is 571-272-1919. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack W. Keith can be reached on 571-272-6878. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JPM
December 9, 2006

Patent Examiner:

Johannes Mondt (Art Unit: 3663)